

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 1. (Currently amended) An apparatus that facilitates implementing a
2 memory mechanism within an asynchronous switch fabric, comprising:
3 a memory device, wherein the memory device has other than first-in, first-
4 out semantics including one of a random access memory and a stack;
5 a data destination horn, for routing data from a trunk line to a plurality of
6 destinations, wherein the memory device is a destination of the plurality of
7 destinations; and
8 a data source funnel, for routing data from a plurality of sources into the
9 trunk line, wherein the memory device is a source of the plurality of sources;
10 wherein the apparatus converts the memory device with other than first-in,
11 first-out semantics to into a dual-port device with first-in, first-out semantics,
12 wherein read/write order hazards are avoided by assigning read and write control to
13 a single port of the dual-port device.

1 2. (Original) The apparatus of claim 1, further comprising:
2 an asynchronous control structure coupled to the data destination horn,
3 that is configured to control propagation of data through the data destination horn;
4 wherein the asynchronous control structure is additionally coupled to the
5 data source funnel, and is additionally configured to control propagation of data
6 through the data source funnel;

7 wherein the asynchronous control structure uses a destination address
8 associated with the data destination horn for the memory device to control
9 propagation of data to the memory device; and
10 wherein the asynchronous control structure uses the destination address for
11 the memory device to control propagation of data from the memory device.

1 3. (Original) The apparatus of claim 2, wherein a read address for the
2 memory device is shared as a write address of the data destination horn for the
3 memory device, so that an order of memory operations for the memory device is
4 identical to an instruction order for the memory device.

1 4. (Original) The apparatus of claim 3, wherein a literal value associated
2 with an instruction for the memory device can specify one of a write operation and
3 a read operation.

1 5. (Original) The apparatus of claim 4, further comprising a first-in, first-
2 out storage structure interposed between the memory device and the data source
3 funnel so that data delivered from the memory device during the read operation
4 will be available to the data source funnel in a same order as delivered from the
5 memory device.

1 6. (Original) The apparatus of claim 1, further comprising:
2 an asynchronous control structure coupled to the data destination horn,
3 that is configured to control propagation of data through the data destination horn;
4 wherein the asynchronous control structure is additionally coupled to the
5 data source funnel, and is additionally configured to control propagation of data
6 through the data source funnel;

7 wherein the asynchronous control structure uses a source address
8 associated with the data source funnel for the memory device to control
9 propagation of data to the memory device; and
10 wherein the asynchronous control structure uses the source address for the
11 memory device to control propagation of data from the memory device.

1 7. (Original) The apparatus of claim 6, wherein a write address for the
2 memory device is shared as a read address of the data source funnel for the
3 memory device, so that an order of memory operations for the memory device is
4 identical to an instruction order for the memory device.

1 8. (Original) The apparatus of claim 7, wherein a literal value associated
2 with an instruction for the memory device can specify one of a write operation and
3 a read operation.

1 9. (Original) The apparatus of claim 8, further comprising a first-in, first-
2 out storage structure interposed between the data destination horn and the memory
3 device so that data delivered from the data destination horn during the write
4 operation will be available to the memory device in a same order as delivered from
5 the data destination horn.

1 10 (Canceled).

1 11. (Currently amended) A computing system that facilitates implementing
2 a memory mechanism within an asynchronous switch fabric, comprising:
3 a memory device, wherein the memory device has other than first-in, first-
4 out semantics including one of a random access memory and a stack;

5 a data destination horn, for routing data from a trunk line to a plurality of
6 destinations, wherein the memory device is a destination of the plurality of
7 destinations; and
8 a data source funnel, for routing data from a plurality of sources into the
9 trunk line, wherein the memory device is a source of the plurality of sources;
10 wherein the apparatus converts the memory device with other than first-in,
11 first-out semantics to into a dual-port device with first-in, first-out semantics,
12 wherein read/write order hazards are avoided by assigning read and write control to
13 a single port of the dual-port device.

1 12. (Original) The computing system of claim 11, further comprising:
2 an asynchronous control structure coupled to the data destination horn,
3 that is configured to control propagation of data through the data destination horn;
4 wherein the asynchronous control structure is additionally coupled to the
5 data source funnel, and is additionally configured to control propagation of data
6 through the data source funnel;
7 wherein the asynchronous control structure uses a destination address
8 associated with the data destination horn for the memory device to control
9 propagation of data to the memory device; and
10 wherein the asynchronous control structure uses the destination address for
11 the memory device to control propagation of data from the memory device.

1 13. (Original) The computing system of claim 12, wherein a read address
2 for the memory device is shared as a write address of the data destination horn for
3 the memory device, so that an order of memory operations for the memory device
4 is identical to an instruction order for the memory device.

1 14. (Original) The computing system of claim 13, wherein a literal value
2 associated with an instruction for the memory device can specify one of a write
3 operation and a read operation.

1 15. (Original) The computing system of claim 14, further comprising a
2 first-in, first-out storage structure interposed between the memory device and the
3 data source funnel so that data delivered from the memory device during the read
4 operation will be available to the data source funnel in a same order as delivered
5 from the memory device.

1 16. (Original) The computing system of claim 11, further comprising:
2 an asynchronous control structure coupled to the data destination horn,
3 that is configured to control propagation of data through the data destination horn;
4 wherein the asynchronous control structure is additionally coupled to the
5 data source funnel, and is additionally configured to control propagation of data
6 through the data source funnel;
7 wherein the asynchronous control structure uses a source address
8 associated with the data source funnel for the memory device to control
9 propagation of data to the memory device; and
10 wherein the asynchronous control structure uses the source address for the
11 memory device to control propagation of data from the memory device.

1 17. (Original) The computing system of claim 16, wherein a write address
2 for the memory device is shared as a read address of the data source funnel for the
3 memory device, so that an order of memory operations for the memory device is
4 identical to an instruction order for the memory device.

1 18. (Original) The computing system of claim 17, wherein a literal value
2 associated with an instruction for the memory device can specify one of a write
3 operation and a read operation.

1 19. (Original) The computing system of claim 18, further comprising a
2 first-in, first-out storage structure interposed between the data destination horn and
3 the memory device so that data delivered from the data destination horn during the
4 write operation will be available to the memory device in a same order as delivered
5 from the data destination horn.

1 20 (Original).

1 21. (Currently amended) A method for implementing a memory
2 mechanism within an asynchronous switch fabric, wherein the memory mechanism
3 is a memory device with other than first-in, first-out semantics including one of a
4 random access memory and a stack, comprising:
5 accepting data from a trunk line to a data destination horn;
6 routing data to a plurality of destinations from the data destination horn,
7 wherein the memory device is a destination of the plurality of destinations;
8 addressing the memory device using a destination address within an
9 asynchronous control structure, wherein the destination address is used to store
10 data in the memory device and to recover data from the memory device;
11 decoding an additional address bit to select one of a memory read and a
12 memory write;
13 providing data to a first-in, first-out storage structure from the memory
14 device;
15 receiving data from the first-in, first-out storage structure at a data source
16 funnel; and

17 applying data from the data source funnel to the trunk line;
18 wherein the method converts the memory device with other than first-in,
19 first-out semantics to into a dual-port device with first-in, first-out semantics,
20 wherein read/write order hazards are avoided by assigning read and write control to
21 a single port of the dual-port device.

1 22. (Currently amended) A method for implementing a memory
2 mechanism within an asynchronous switch fabric, wherein the memory mechanism
3 includes a memory device with other than first-in, first-out semantics, comprising:
4 accepting data from a trunk line to a data destination horn;
5 routing data to a plurality of destinations from the data destination horn,
6 wherein a first-in, first-out storage structure is a destination of the plurality of
7 destinations;
8 providing data to the memory device from the first-in, first-out storage
9 structure;
10 addressing the memory device using a source address within an
11 asynchronous control structure, wherein the source address is used to store data in
12 the memory device and to recover data from the memory device;
13 decoding an additional address bit to select one of a memory read and a
14 memory write;
15 receiving data from the memory device at a data source funnel; and
16 applying data from the data source funnel to the trunk line;
17 wherein the method converts the memory device with other than first-in,
18 first-out semantics to into a dual-port device with first-in, first-out semantics,
19 wherein read/write order hazards are avoided by assigning read and write control to
20 a single port of the dual-port device.